REMARKS

The Office Action dated July 27, 2007 has been received and considered. In this response, claims 13, 15, 44, 52, and 53 have been amended and claim 14 has been canceled without prejudice or disclaimer. Support for the amendments may be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 13-29, 31-40, 43-50, 52 and 53

At page 2 of the Office Action, claims 13-29, 31-40, 43-50, 52 and 53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eifrig (U.S. Patent No. 6,748,020 B1). This rejection is respectfully traversed with amendment.

Under 35 U.S.C. § 103, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Office can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of references. *Id.*

Obviousness of Separate Processors

Independent claims 13, 44, and 53 recite subject matter directed to a first processor and a second processor and their respective functionality/operations. For each of claims 13, 44, and 53, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. *See Office Action*, pp. 2, 5, and 6. As discussed in greater detail at pages 9-12 of the Response filed May 7, 2007 (hereinafter, "the Previous Response"), the Office's interpretation of element 10 and element 30 of Eifrig as two separate processors is suggested solely by the Present Application. Nowhere does Eifrig disclose that element 10 and element 30 each are implemented as a separate processor. In fact, Eifrig expressly teaches that element 10 and element 30 are implemented at the same Very Long Instruction Word (VLIW) core. *See, e.g., Eifrig*, col. 4, lines 6-33 ("a) MPEG transport stream

decoding (on VLIW core)(10) [. . .] c) Core transcoding (on VLIW core)(30) [. . .]")(emphasis added). As also discussed in the Previous Response, one of ordinary skill in the art will recognize that the parsing/demux (element 10) and the corresponding core transcoder (element 30) conventionally are implemented together as a single processor.

The Office responds by acknowledging that Eifrig "does not particularly disclose that a first element and a second element are different processors as specified in claims 13, 44, and 53." The Office then reasons that "[i]t would have been obvious to one ordinary skilled [sic] in the art at the time the invention was made to make the VLIW processor of Eifrig et al separable since the mere fact that a given structure does not preclude its consisting of various elements (Nerwin v. Erlichman, 168 USPQ 177, 179 (PTO Bd. of Int. 1969) and *doing so would help speed up the transcoding process*." *Office Action*, p. 6 (emphasis added).

While the Applicants can understand the Office's temptation to find the holding in Nerwin v. Erlichman applicable to the Present Application, the facts in dispute in Nerwin v. Erlichman are not the same as or analogous to those in the Present Application. At issue in Nerwin was whether the integral guide member 198 of a film roll processing apparatus disclosed by Erlichman can constitute the two separate elements claimed by Nerwin, namely "a divider between said exposure and processing chamber" and "means effective upon movement of said strip along for directing the leading edge of each said sheet. . . ." *See Nerwin*, pp. 178-179. Thus, the issue before the Board of Interferences was whether a single mechanical component of Erlichman can be said to disclose two separate mechanical components claimed by Nerwin. It is one thing to find it obvious that an integral mechanical component can be interpreted as comprising multiple mechanical elements. *See Howard et al. v. Detroit Stove Works*, 150 U.S. 164, 65 O.G. 1765 1893 C.D. 659. It is completely another to find it obvious to separate the complex circuitry as would be found in the VLIW processor of Eifrig into separate processors at least due to a variety of complicating factors, such as signaling issues, timing issues, communication issues, footprint issues, power issues, and the like. In view of the complexity of this task, there would need to be some motivation to make such efforts. Thus, the issue in the Present Application is not whether a single integral mechanical element can disclose two distinct mechanical elements but rather whether one of ordinary skill would be obvious to implement

certain complex and non-trivial processing functionality implemented into separate processors in the manner recited by independent claims 13, 44, and 53.

As discussed above and in the Previous Response, the functionality recited by the claims conventionally is implemented in a single processor, such as the VLIW processor disclosed by Eifrig. The Office fails to provide a prior art reference showing that it was contemplated or was otherwise known in the video processing arts to separate video processing functions into separate processors. Further, although the Office asserts that it would have been obvious to do so "to help speed up the transcoding process," it is noted that no reference has been offered by the Office to demonstrate that the separation of functionality into different processors as recited by the claims would speed up the transcoding and thus the Office fails to provide *any* evidence as to the veracity of this assertion. *See Office Action*, p. 6. In fact, the only evidence of this advantage is provided by the disclosure of the Present Application itself. *See, e.g., Present Application*, p. 5, lines 1-8. Accordingly, the Office fails to meet its burden of establishing a *prima facie* case that the implementation of video processing functionality in two processors as recited by the pending claims would have been obvious in view of Eifrig.

Eifrig fails to disclose or suggest each and every feature recited by claims 13, 44 and 53

Independent claim 13 has been amended and presently recites the features of "a memory", "a first processor to parse received video data to generate a plurality of packets and provide the plurality of packets for storage in the memory, the first processor comprising a general purpose processor," and "a second processor to access packets of the plurality of packets from the memory, the second processor including a video transcoder to transcode video data of the packets." The Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and further that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. As discussed above, one of ordinary skill in the art will recognize that the parsing/demux (element 10) and the corresponding core transcoder (element 30) conventionally are implemented together as a single processor and the Office fails to establish that it would have been obvious to implement these elements in separate processors as provided by claim 13.

Further, claim 13 provides that the first processor is to parse received video data to generate a plurality of packets and provide the plurality of packets to the memory. Eifrig fails to disclose that its element 10 (which the Office equates to the claimed first processor) packetizes video data into packets and then stores the packets in memory. Claim 13 also provides that the second processor is to access packets from the memory and includes a transcoder to transcode the packets. Eifrig fails to disclose or suggest that the element 30 accesses packets from memory for transcoding. Claim 13 also provides that the first processor is a general purpose processor, where the present application provides that "[a] general purpose processor is a data processor that performs one or more functions specified by software, where it is understood that software would include firmware." *Present Application*, p. 10, lines 29-31. Other than merely asserting that element 10 "is a general purpose element," the Office fails to establish that Eifrig teaches that the element 10 is a general purpose processor. *See Office Action*, p. 2. Eifrig provides no disclosure that the parsing/demux element (element 10) "performs one or more functions specified by software." Moreover, one of ordinary skill in the art would appreciate that the element 10 of Eifrig would be implemented solely as hardware (e.g., a state machine) rather than as a general purpose processor. For at least the reasons provided above, it is respectfully submitted that Eifrig fails to disclose or suggest each and every feature recited by claim 13.

Independent claim 53 recites the features of: "receiving, at a first processor, a data stream including video data," "parsing, *at the first processor*, the data stream to identify video data associated with a first channel," "packetizing, *at the first processor*, the video data associated with the first channel to generate the one or more packets, each packet having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristics represented by a first value," "*storing the one or more packets at a memory*", "*accessing*, at a second processor, the one or more packets *from the memory*," and "transcoding, *at the second processor*, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value." As with claim 13, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the first processor at which the claimed receiving, parsing, and packetizing operations are performed, and further that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the second processor at which the claimed

receiving and transcoding operations are performed. However, as discussed above with respect to claim 13, the Office's interpretation of element 10 and element 30 of FIG. 1 of Eifrig as two separate processors is suggested solely by the present application and finds no support in the disclosure of Eifrig or in the knowledge of one of ordinary skill in the art at the time of the invention. Further, Eifrig fails to disclose or suggest the element 10 packetizes the video data and stores the packets in a memory, or that the element 30 accesses the packets from the memory as provided by claim 53. Accordingly, Eifrig fails to disclose or suggest the above-identified features of claim 53.

Independent claim 44 has been amended and presently recites the features of "a *memory*", "a first data processor to: *access one or more packets* having a video data payload and information related to the video data payload *from the memory*, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value; and transcode the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value" and "*a second data processor comprising a general purpose processor*, the second data processor to: receive a data stream including video data at a first data processor; parse the data stream to identify video data associated with a first channel; packetize the video data associated with the first channel to generate the one or more packets; and *provide the one or more packets for storage in the memory*." As discussed above, Eifrig fails to disclose or suggest one data processor to parse and packetize video data and a separate processor to transcode the parsed and packetized video data. Eifrig also fails to disclose or suggest that the element 10 stores packets in memory and that the element 30 accesses the packets from memory for processing. Eifrig therefore fails to disclose or suggest the claimed first and second data processor features recited by claim 44.

Eifrig fails to disclose or suggest a second processor coupled to a first processor through a memory controller and a sequencer as recited by claim 29

Dependent claim 29 recites the features of "wherein the second processor is coupled to the first processor through a memory controller and a sequencer." With respect to these features, the Office merely states "wherein the second element is coupled to the first element through a memory controller and a sequencer (el. 10 and 20) as specified in claim 29" and provides no

further support for its rejection of claim 29. *Office Action*, p. 3. From this statement, it is unclear as to whether the Office is associating elements 10 and 20 of Eifrig with the recited first and second processors or with the recited memory controller and sequencer. If the Office intended the former, then it is submitted that the Office fails to establish how Eifrig discloses a memory controller and a sequencer (much less that they couple two processors) and thus the Office fails to meet its burden of establishing a *prima facie* case of obviousness with respect to claim 29. If the Office instead intended the latter, that is, that the memory controller and sequencer of claim 29 are met by elements 10 and 20 of Eifrig, it is submitted that the Office identifies element 10 also as the first processor, so it is not understood how a first processor (allegedly element 10) can be coupled to a second processor through itself (allegedly through elements 10 and 20). Moreover, it is not understood how elements 10 and 20 constitute a memory controller and a sequencer.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-1835.

Respectfully submitted,

/Ryan S. Davidson/ November 20, 2007

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